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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,424	07/12/2002	Kwun-Yao Ho	9407-US-PA	9331

31561 7590 10/20/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,424	HO ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (Claims 1-9) in the reply filed on October 01, 2004 is acknowledged. The Examiner acknowledges the cancellation of non-elected Claims 10-27.

Claim Objections

2. Claims 3-9 are objected to for the following reasons:

(i) Claims 3 and 4 fail to particularly point out and distinctly claim the subject matter which applicant regards as the invention as required in 37 CFR § 1.75(a). Specifically:

(a) Claim 3 recites the limitation "the via opening layer" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. The objection may be easily overcome by changing the dependency of Claim 3 from "claim 1" to -- claim 2-- in line 1 of the claim.

(b) Claim 4 recites the limitation "the via opening layer" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. The objection may be easily overcome by changing the dependency of Claim 4 from "claim 1" to -- claim 2-- in line 1 of the claim.

(c) Claim 5 recites the limitation "the via holes" in line 5, and "the via holes in the two most exterior dielectric layers" in line 6. There is insufficient antecedent basis for *the via holes* in the claim. The Examiner will interpret Claim 5 in

accordance with the following proposed amendment recommended to overcome the objection:

In line 5: change "via holes" to --via studs--.

In line 6: change "via holes to --via studs--.

(ii) In Claim 4, line 1: "whether" should be changed to --wherein--.

(iii) In Claim 9, line 1: "whether" should be changed to --wherein--.

(iv) Claims 6-9 depend from defective Claim 5 and therefore inherit the above-cited defects of the claim.

Appropriate correction is required.

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

Frankeny et al. (US 5,146,674) Hurwitz et al. (US 6,262,376 B1)

Frankeny et al. (US 5,121,299) Miura et al. (US 5,768,108)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Hurwitz et al.

Hurwitz et al. discloses, in Fig. 1: a laminated substrate structure 10, wherein structure 10 comprises a plurality of dielectric layers 18 and a plurality of circuit layers 14, 16, 17 and 19 stacked with each other, each of the dielectric layers 18 has a plurality of via studs 24, and the circuit layers 14, 16, 17 and 19 are electrically coupled with each other through the via studs 24 (col.5: 54-55), the laminated substrate structure 10 is characterized by a pattern of circuit layers 14, 16, 17 and 19 designed as landless (col.2: 63-col.3: 8; col.5: 14-17).

6. Claims 1, 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Frankeny et al. (US 5,146,674).

As to Claim 1, Frankeny et al. (US 5,146,674) discloses a laminated substrate structure 55, in Fig. 24, wherein the structure comprises a plurality of dielectric layers 21 (col.5: 1-7) and a plurality of circuit layers 35 (col.5: 53-55) stacked with each other, each of the dielectric layers has a plurality of via studs (17, 17a) (Figs. 7-22) and 57 (col.8: 5-8 and 22-26), and the circuit layers 35 are electrically coupled with each other through via studs (17, 17a, 57) the laminated substrate structure 55 is characterized by a pattern of circuit layers 35 designed as landless (Fig. 24; the connections between metallized dielectric layers 21 are directly through the via studs with joined by the solder layers 43 and 49; see Figs. 18, 19, 22, 23 and 24 in sequence and col.6: 11-18; there are clearly no interconnection lands in the structure of Fig. 24, hence, a pattern of circuit layers 35 is designed as landless).

As to Claim 5, Frankeny et al. (US 5,146,674) discloses a laminate substrate structure 55, in Fig. 24, comprising: a plurality of dielectric layers 21 (col.5: 1-7), each of the dielectric layers 21 has a plurality of via studs (17, 17a) (Figs. 7-22) and 57 (col.8: 5-8 and 22-26); a plurality of circuit layers 35 (col.5: 53-55), arranged in between the dielectric layers 21, the circuit layers 35 are electrically coupled to each other through the via studs (17, 17a, 57), wherein the via studs 57 and (17, 17a) in the two most exterior dielectric layers 21 are used as a plurality of solder pads directly (via stud 57 is used as a solder pad for joining material 67 and solder ball 65, as taught in col.8: 22-31; and bottom via stud 17; 17a is used as a solder pad for the solder connection to another dielectric layer 21, a component, or a circuit board [not shown in Fig. 24], said solder layer on via stud 17, 17a is seen in Fig. 24 and described as solder layer 43 in Fig. 15 and col.6: 11-15 and 22-24).

As to Claim 6, Frankeny et al. (US 5,146,674) further discloses a pattern of the circuit layers 35 is designed as landless (Fig. 24; the connections between metallized dielectric layers 21 are directly through the via studs with joined by the solder layers 43 and 49; see Figs. 18, 19, 22, 23 and 24 in sequence and col.6: 11-18; there are clearly no interconnection lands in the structure of Fig. 24, hence, a pattern of the circuit layers 35 is designed as landless).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US 5,146,674) in view of Miura et al.

As to Claims 2 and 7:

I. Frankeny et al. (US 5,146,674) discloses all the limitations of base Claims 1 and 5, respectively, and further discloses at least a via opening layer 61 arranged on one (i.e., the topmost) of the two most exterior dielectric layers 21 for the purpose of allowing IC chip 63 with solder balls 65 to be pressed into place on the laminate substrate surface with a greater amount of force to ensure reliable electromechnical connection to the substrate (Fig. 24; col.8: 32-36).

II. Frankeny et al. (US 5,146,674) does not teach that the exterior dielectric layer 21 on the bottom of the laminate substrate also has a via opening layer for mounting another IC chip 63 with solder balls 65.

III. Miura et al. discloses a laminate substrate having landless via studs, i.e., filled-in through-holes (Fig. 10; col.7: 41-43; col.11: 55-59) and further discloses IC chips 42 with bumps solder balls 41 (Fig. 10; col.12: 4-7) mounted on both sides of the laminate substrate (IC chips 68 and 69 in Fig. 13; col.12: 44-45 and col.13: 5-10) in order to increase the functionality of the laminate structure as required by an electronic application.

IV. Since both Frankeny et al. (US 5,146,674) and Miura et al. are both in the art of packaging chips onto a landless via stud laminate, then the increase in functionality

effected by a double-sided laminate substrate that mounts IC flip chips on both sides of the substrate, as taught by Miura et al., would have been readily recognized as a functionally beneficial modification in the pertinent art of Frankeny et al. (US 5,146,674).

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the exterior bottom dielectric layer 21 in Frankeny et al. (US 5,146,674) such that it has arranged thereon a via opening layer 61 that is the same as the via opening layer 61 on the exterior top dielectric layer 21 of Frankeny et al. (US 5,146,674) in order to modify the laminate substrate 55 of Frankeny et al. (US 5,146,674) so that it is a double-sided substrate that mounts IC flip chips 63 on both sides of the substrate in order to upgrade the functionality of the package to meet the demands of an electronic application, as taught by Miura et al.

9. Claims 3-4 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US 5,146,674) in view of Miura et al., as applied, respectively, to Claims 2 and 7 above, and further in view of Frankeny et al. (US 5,121,299).

As to Claims 3-4 and 8-9, modified Frankeny et al. (US 5,146,674) further discloses that via opening layer 61 is a dielectric layer, and the dielectric layer has a plurality of openings; specifically, the dielectric via opening layer 61 is a solder mask layer (Fig. 24; col.8: 32-38). Also, **see Fig. 13 and col.4: 27-34 in Frankeny et al. (US 5,121,299)**--which is the patent that matured from the US patent application 07/459,087 that is referenced in col.8: 36-38 of Frankeny et al. (US 5,146,674)--wherein the via opening layer 61 of Frankeny et al. (US 5,146,674) is disclosed in Frankeny et al. (US 5,121,299; Fig. 13 and col.4: 27-34) as a dielectric solder mask layer.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) The following references disclose a landless laminated substrate structure with via studs:

Smith et al. (US 5,287,619): Fig. 34; col.3: 1-6 and 15-17.

Andou et al. (US 6,197,407 B1): Fig. 7; col.2: 37-42; col.9: 31-41; col.18: 6-10.

Sachdev et al. (US 5,231,751): Fig. 15 ; col.9: 18-22 and 28-41.

b) Kambe et al. (US 6,323,439 B1) discloses, in Fig. 3G, a laminated substrate structure having via studs 45, 46 and 47 and lands, and further including a via hole layer--i.e., dielectric layer 61 and 62--arranged on each of the two most exterior dielectric layers 41 and 42, respectively, of the laminated substrate structure (col.11: 23-30).

c) Watanabe et al. (US 6,326,561 B1) discloses a laminated substrate structure 24 having via studs 3 and lands formed directly on the via stud surface to receive the via studs 3 of the next laminar layer (Figs. 6A-G, 7 and 10; col.4: 30-37; col.5: 42-48; col.7: 11-22).

d) Murakami (US 5,092,032) discloses a via stud 5 used as a solder pad for solder 9, whereby electronic component 10 is mounted to the substrate (Figs. 1G and 1H; col.6: 42-51).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
October 16, 2004